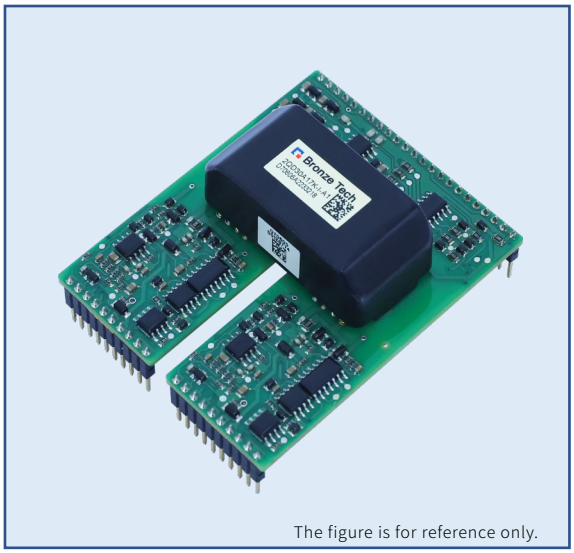
2QD30A17K-I-xx Gate Driver Core



The figure is for reference only.

Features

RoHS COMPLIANT

- Dual-channel IGBT gate driver core
- Blocking voltage up to 1700V
- Peak current ±30A, 4W output power per channel
- Up to 6000V isolation voltage
- Direct/half-bridge mode available
- Secondary side undervoltage lockout
- IGBT short-circuit protection integrated
- Active clamping integrated
- Soft shut down integrated
- UL94V-0 compliant materials

KEY PARAMETERS	
V_{CC}, V_{DC}	15V
V_G	+15.4V, -15.7V
P, MAX	4W
I_G, MAX	±30A
f_S, MAX	60kHz
T_A	-40°C ~85°C
Isolation Voltage	6000Vac

Description

2QD30A17K-I-xx is a high power, dual-channel compact gate driver core designed for high reliability applications.

2QD30A17K-I-xx can be used for IGBT modules with a blocking voltage up to 1700V. It can be applied to various topologies by adding proper peripheral circuitry.

Typical Applications

- Engergy storage converters
- Wind power converters
- PV inverters

Block Diagram

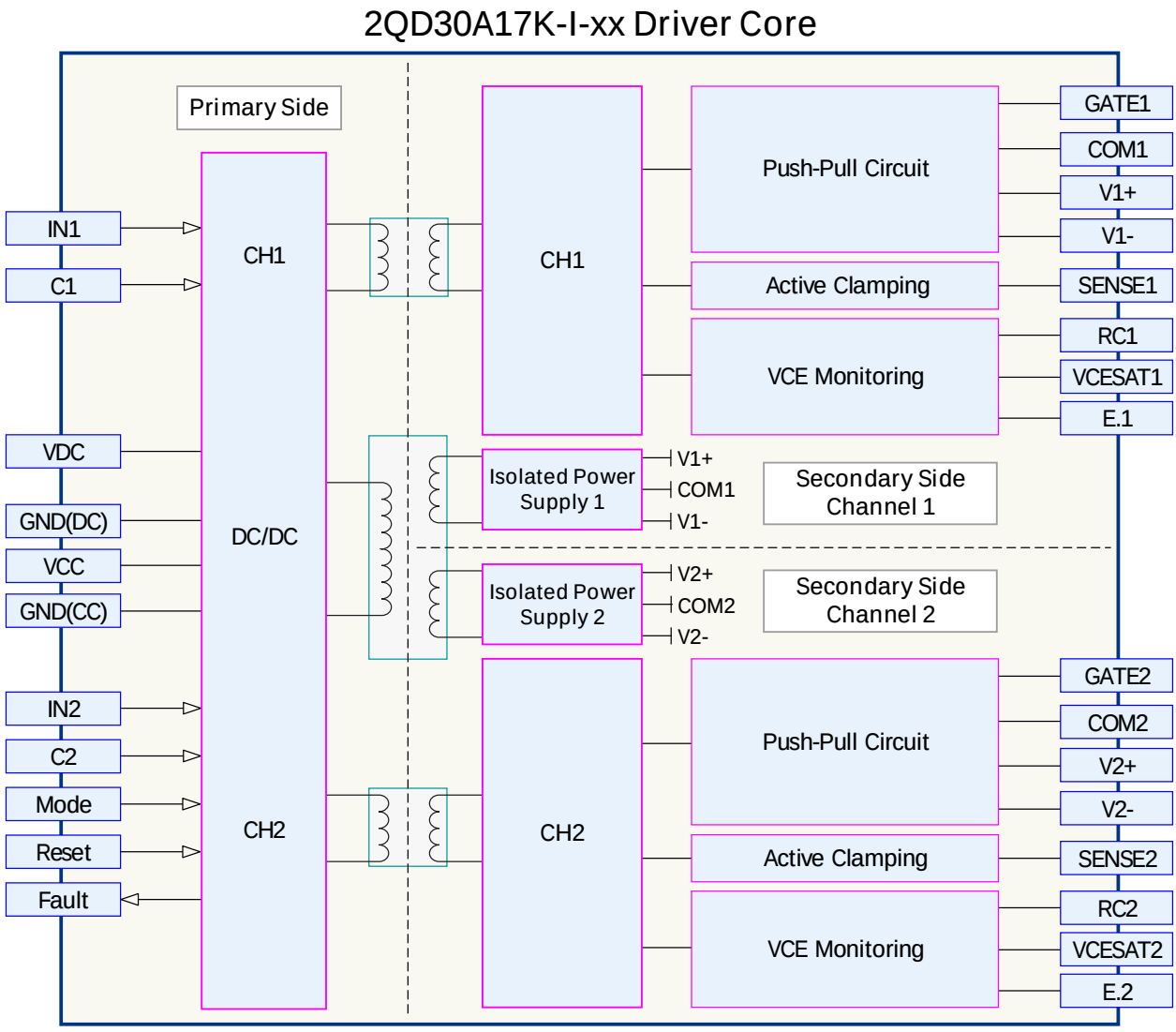


Figure 1. Block diagram of the driver core 2QD30A17K-I-xx

Recommended Circuitry

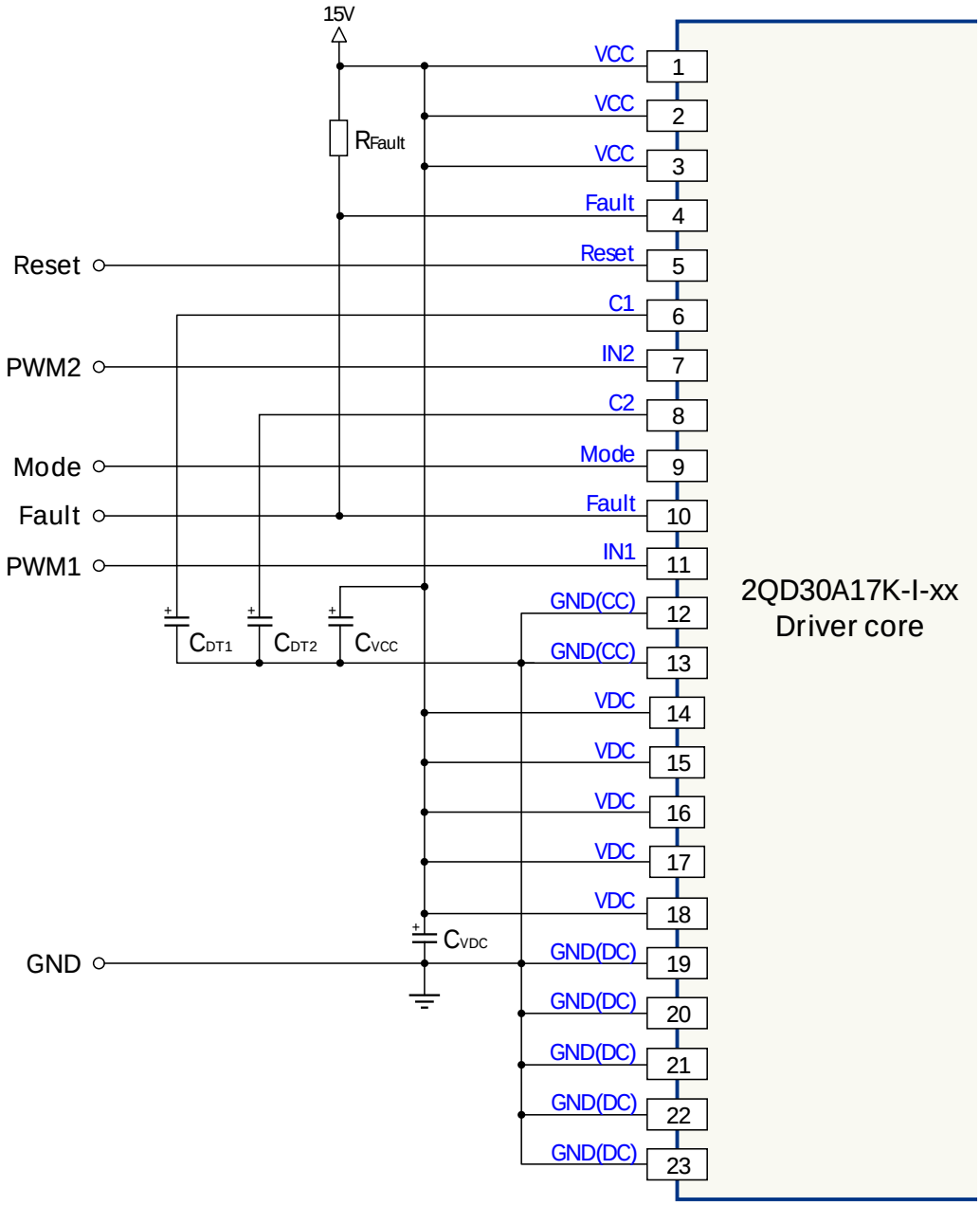


Figure 2. Recommended user interface of 2QD30A17K-I-xx (Primary side)

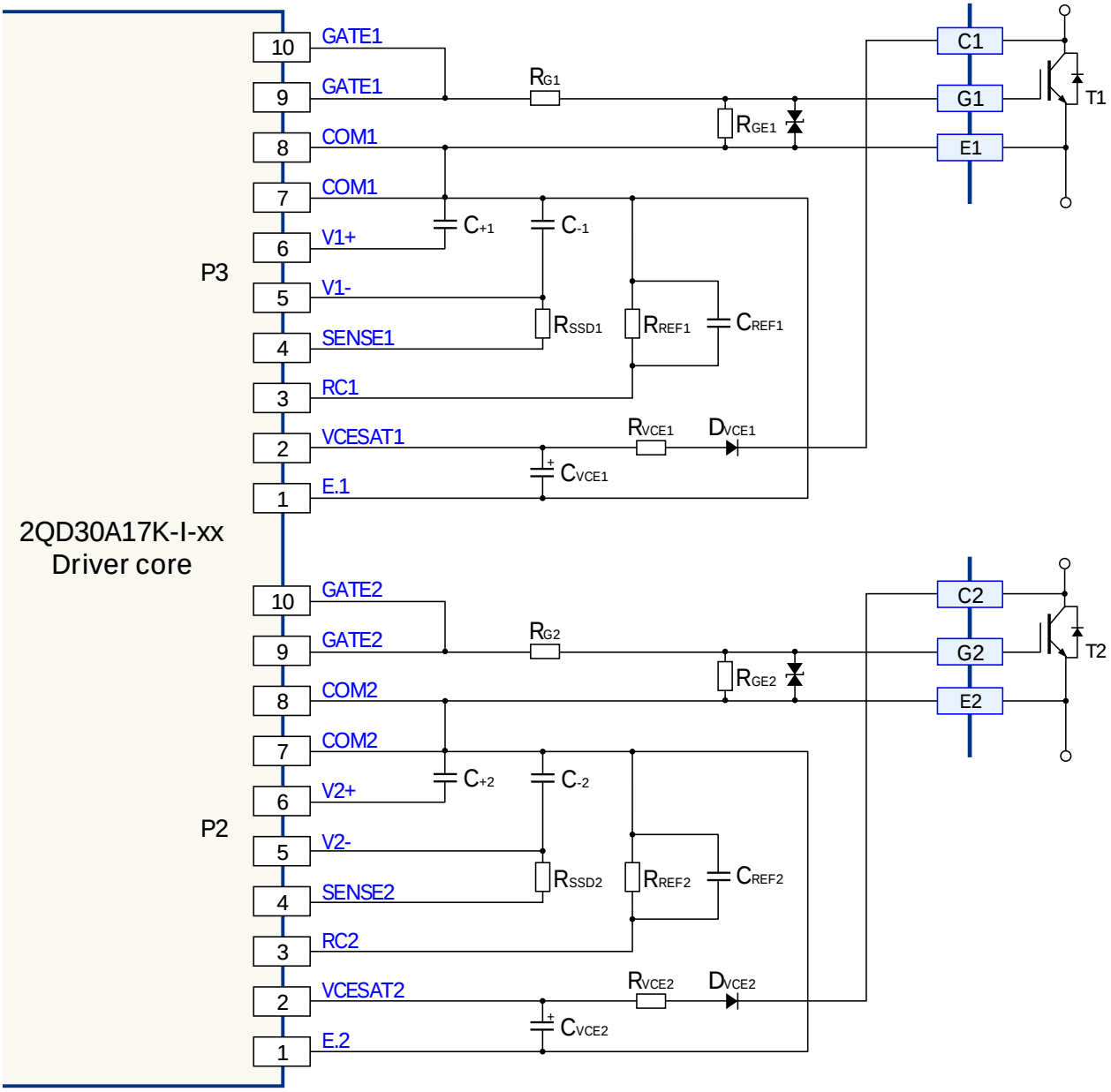


Figure 3. Recommended user interface of 2QD30A17K-I-xx (Secondary side)

Pin Designation

P1 Terminal

Pin	Symbol	Description	Pin	Symbol	Description
1	VCC	15V for primary side electronics	13	GND(CC)	Signal ground
2	VCC	15V for primary side electronics	14	VDC	15V for DC/DC converter
3	VCC	15V for primary side electronics	15	VDC	15V for DC/DC converter
4	Fault	Open collector fault output	16	VDC	15V for DC/DC converter
5	Reset	Logic reset input, active high	17	VDC	15V for DC/DC converter
6	C1	External capacitor terminal for half-bridge mode dead time adjustment channel 1	18	VDC	15V for DC/DC converter
7	IN2	Signal input channel 2	19	GND (DC)	Power ground
8	C2	External capacitor terminal for half-bridge mode dead time adjustment channel 2	20	GND (DC)	Power ground
9	Mode	Mode selection (direct/half-bridge mode)	21	GND (DC)	Power ground
10	Fault	Open collector fault output	22	GND (DC)	Power ground
11	IN1	Signal input channel 1	23	GND (DC)	Power ground
12	GND(CC)	Signal ground			

P2 Terminal

Pin	Symbol	Description	Pin	Symbol	Description
1	E.2	External digital fault input driver channel 2	6	V2+	External capacitor terminal for positive power supply driver channel 2
2	VCESAT2	IGBT desaturation sensing input driver channel 2	7	COM2	Common ground terminal driver channel 2
3	RC2	Desaturation reference curve RC network terminal driver channel 2	8	COM2	Common ground terminal driver channel 2
4	SENSE2	Active clamping input or soft shut down resistor terminal driver channel 2	9	GATE2	IGBT gate output driver channel 2
5	V2-	External capacitor terminal for negative power supply driver channel 2	10	GATE2	IGBT gate output driver channel 2

P3 Terminal

Pin	Symbol	Description	Pin	Symbol	Description
1	E.1	External digital fault input driver channel 1	6	V1+	External capacitor terminal for positive power supply driver channel 1
2	VCESAT1	IGBT desaturation sensing input driver channel 1	7	COM1	Common ground terminal driver channel 1
3	RC1	Desaturation reference curve RC network terminal driver channel 1	8	COM1	Common ground terminal driver channel 1
4	SENSE1	Active clamping input or soft shut down resistor terminal driver channel 1	9	GATE1	IGBT gate output driver channel 1
5	V1-	External capacitor terminal for negative power supply driver channel 1	10	GATE1	IGBT gate output driver channel 1

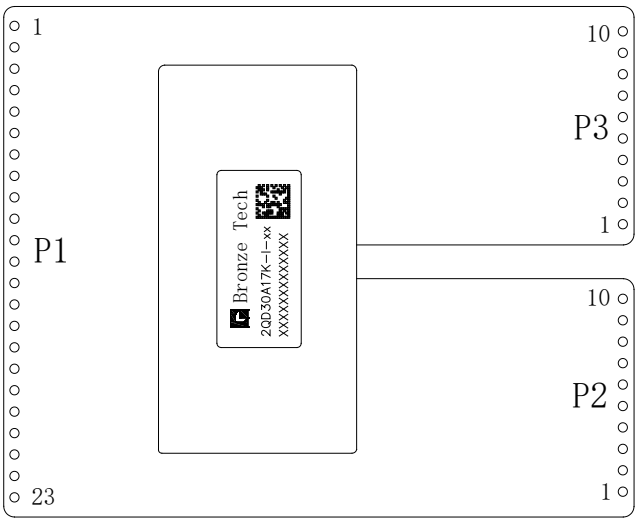


Figure 4. 2QD30A17K-I-xx Pin layout

Specifications

Absolute Maximum Ratings

PARAMETER	REMARKS	MIN	MAX	UNIT
Supply voltage V_{CC}, V_{DC}	VCC, VDC to GND	0	16	V
Logic input voltages	Primary side, to GND	0	15	
Logic output voltage	Primary side, to GND	0	VCC	
Total fault output current on one or both terminals			40	mA
Output power per channel	Operating termperature ⩽ 85°C		4	W
Gate peak current [1)]		-30	30	A
External gate resistance		1		Ω
IGBT gate charge			52	μC
Operating voltage			1700	V
Average supply current I_{CC}+I_{DC} [2)]			680	mA
Switching frequency			60	kHz
Operating temperature T_A		-40	85	°C
Storage temperature T_S		-40	85	

Note: 1. It is an absolute value and only valid for short pulses.
2. The average current may exceed the specified maximum value during transient (e.g. power supply start up).
This short overload is allowed as long as the temperature rise after the transient does not exceed the thermal limitation.

Power supply and monitoring

Operating temperature T_A=25°C , V_{CC}=V_{DC}=15V, unless otherwise specified, tested along with the recommended interface circuitry.

PARAMETER		TEST CONDITONS	MIN	TYP	MAX	UNIT
Supply voltage V_{CC}, V_{DC}		VCC, VDC to GND,	14	15	16	V
Supply current I_{DC}		No load, f_{SW}=0Hz		89		mA
Supply current I_{DC}	R_G=1Ω	No load, f_{SW}=5kHz, 50% duty cycle		111		
		No load, f_{SW}=10kHz, 50% duty cycle		114		
		Load capacitance 100nF, f_{SW}=10kHz, 50% duty cycle		250		
Secondary-side full voltage V_{CCO}		Vx+ to Vx-, no load		32		V
Secondary-side positive voltage V+		Vx+ to COMx, no load		16		
Secondary-side negative voltage V-		Vx- to COMx, no load		-16		
Secondary side positive supply UVLO threshold voltage [1)]	Set fault V_{UV+}	Vx+ to COMx		10.6		V
Secondary side negative supply UVLO threshold voltage [1)]	Set fault V_{UV-}	Vx- to COMx		-10.9		

Note: 1. See section "Power Supply and Monitoring" for timing diagram of the UVLO.

Logic Input and Output

Operating temperature T_A=25°C , V_{CC}=V_{DC}=15V, unless otherwise specified, tested along with the recommended interface circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IN1, IN2 Input voltage V_{IN}	Turn-on threshold V_{INH}			8.0		V
	Turn-off threshold V_{INL}			5.7		
Fault output votlage V_{Fault} 1)	Normal state	R_{Fault}=2.2kΩ pulled up to VCC		15		V
	Blocking state	I_{Fault} < 40mA			0.6	
Input threshold for external failure input E.x 2)				5.1		V

Note: 1. Fault output has open-collector transistors, users need to add the pull-up resistor R_{Fault} externally.
For more details see the section "Status Output Signal".
2. If not used, E.x should be shorted to COMx.

Gate Drive Output

Operating temperature T_A=25°C , V_{CC}=V_{DC}=15V, unless otherwise specified, tested along with the recommended interface circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage V_{Gx}	ON-State GATEx to COMx	No load		15.4		V
		Output power 4W		14.2		
	OFF-State GATEx to COMx	No load		-15.7		
		Output power 4W		-14.5		
Gate peak current $I_{G\ peak}$	Source current	R_G=1Ω			30	A
	Sink current		-30			
Blocking capacitance for V+, on board 1)		Vx+ to COMx		7.5		µF
Blocking capacitance for V-, on board 1)		COMx to Vx-		7		

Note: 1. External blocking capacitors are required to be placed between Vx+ and COMx as well as between COMx and Vx-, 220µF is recommended.

Short Circut Protection

Operating temperature T_A=25°C , V_{CC}=V_{DC}=15V, unless otherwise specified, tested along with the recommended interface circuitry.

PARAMETER	TEST CONDITONS	MIN	TYP	MAX	UNIT
V_{CE} monitoring threshold V_{REF}		2		9	V
Transmission delay of fault state t_{SO} 2)	Secondary-side short-circuit protection action to fault status output		2.2		µs

Note: 1. The diode detection method is used for test. R_{REFx}/C_{REFx} are on the external mother board.
For response time configuration, see the section "IGBT Short Circuit Protection".
2. Propagation delay time is from the secondary-side protection action to the primary-side Fault pin pulled down.

Timing Characteristics

Operating temperature T_A=25°C , V_{CC}=V_{DC}=15V, unless otherwise specified, tested along with the recommended interface circuitry.

PARAMETER		TEST CONDITONS	MIN	TYP	MAX	UNIT
Propagation delay [1) 3)]	Turn-on delay $t_{d(on)}$	Mode pin shorted to GND, R_G=1Ω, no load		596		ns
	Turn-off delay $t_{d(off)}$			585		
Jitter of turn-on delay		R_G=1Ω, no load		±8.3		
Jitter of turn-off delay				±9.8		
Output rise time t_r [2) 3)]				99		
Output fall time t_f [2) 3)]				79		
Dead time DT [4)]		Half-bridge mode, Mode pin shorted to VCC, C_{DTx}=0		1.6		µs
Jitter of dead time					±11	ns

Note: 1. The delay time is measured between 50% of the input signal and 10% (90%) voltage swing of V_{Gx}.
The delay time is independent of the output load.
2. Output rise (fall) time is measured at GATEx between the 10% and 90% of the nominal voltage swing. The time constant of the output load capacitance in conjunction with the present gate resistors leads to an additional delay at the load side of the gate resistors.
3. The voltage swing is the diffrerence between the output voltage at ON and OFF state on the GATEx pin, referred to COMx.
4. For dead time configuration see section "Transmission Logic and Mode Selection / Half-Bridge Mode ".

Electrical Isolation

Operating temperature T_A=25° C, unless otherwise specified, tested along with the standard peripheral circuitry.

PARAMETER		VALUE	UNIT
Isolation voltage (50Hz, 1s, RMS value)	Primary to Secondary side	6000	V
	Secondary to Secondary side	4000	
Primary to secondary side [1)]	Coupling capacitance	20	pF
	Clearance distance	21	mm
	Creepage distance	21	
Secondary to secondary side [1)]	Coupling capacitance	9	pF
	Clearance distance	8.5	mm
	Creepage distance	15	

Note: 1. Clearance and creepage distances are designed according to IEC 61800-5-1.

EMC

PARAMETER		VALUE	UNIT
ESD immunity (IEC 61000-4-2)	Contact discharge	±4	kV
	Air discharge	±8	
Electrical fast transient/burst immunity [1] (IEC 61000-4-4)		±3	
Note: 1. Tested on power ports.			

Ordering Information

Part Number	Pin Length	With Fuse at Secondary Side power supply or not	Conformal Coating
2QD30A17K-I-A0	5.8mm	No	Yes
2QD30A17K-I-A1	5.8mm	Yes	Yes
2QD30A17K-I-C0	3.0mm	No	Yes
2QD30A17K-I-C1	3.0mm	Yes	Yes

Function Description

Power Supply and Monitoring

The DC/DC circuitry of the driver provides galvanic isolation between external power supply and gate driving circuit.

Supply monitoring circuitry is deployed for two secondary-sides of the driver for undervoltage lockout.

Note: VDC pin supplies the DC/DC while VCC pin supplies the logic circuitry. GND(DC) and GND(CC) must be connected together to the ground on the user's mother board.

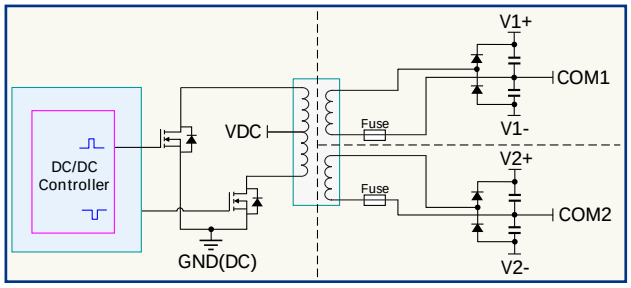


Figure 5. Power supply circuitry, secondary side power supply with fuse

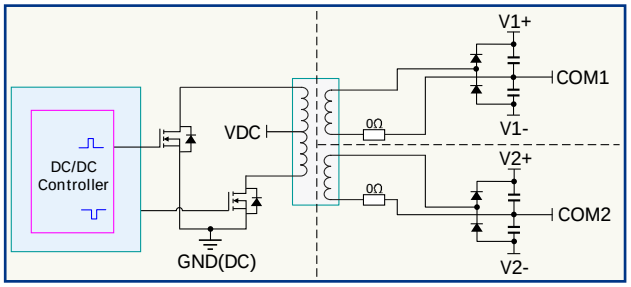


Figure 6. Power supply circuitry, secondary side power supply without fuse (replaced by 0Ω resistor)

The secondary power supply voltage is also monitored to ensure a safe IGBT switching. To demonstrate the behavior of the secondary side UVLO, a scenario is considered in below where the primary side supply voltage V_{DC} decreases from the nominal value towards zero:

1) When V+ or V- reaches the set fault threshold V_{UV+} or V_{UV-}, UVLO protection is initiated. The IGBT is turned off and held in off state, meanwhile a set fault signal is transmitted to the primary side and asserts Fault pin immediately.

2) When V_{DC} rises again, V+ and V- recover, as both reaches their clear fault threshold V_{UV+} or V_{UV-}, the driver circuitry still remains inactive. Only after Reset signal is asserted, the driver resumes operation and Fault signal is cleared.

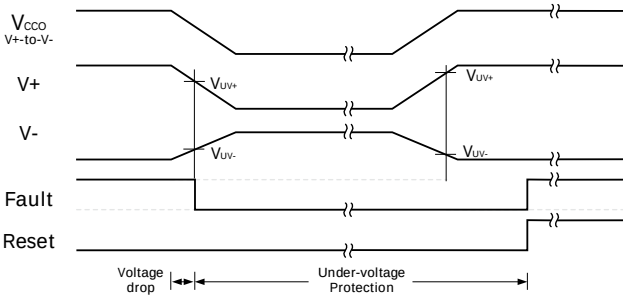


Figure 7. UVLO Logic

Input Signal

The PWM signal is input from INx pin. Pulses shorter than 320ns from INx is suppressed, where the driver output will not react to it.

The Reset pin is used to resume the driver output by a logic high after fault clearance. The resume can be also achieved by keep IN1 and IN2 low for more than 50ms.

Transmission Logic and Mode Selection

The driver can operate in direct or half-bridge mode. Operating mode of the driver can be selected by configuring the connection of the Mode pin.

Direct Mode:

If the Mode pin is shorted to GND(CC), direct mode is selected. In direct mode, the two channels are independent. Input IN1 determines the output of Channel 1, while input IN2 determines that of Channel 2. A logic high turns on the corresponding IGBT, while a logic low turns it off.

Note: In direct mode, make sure to add a proper dead time in the input signals to avoid shoot-through of the two switches in a bridge.

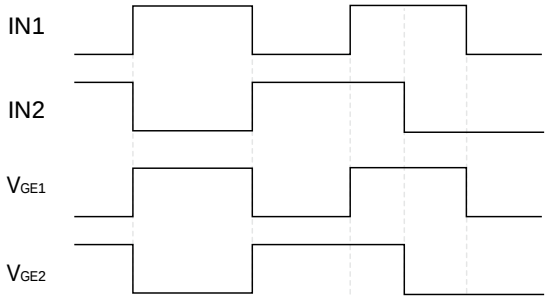


Figure 8. Transmission logic in direct mode

Half-Bridge Mode:

If the Mode pin is connected to V_{CC}, the driver operates in half-bridge mode. When IN1 goes from high to low, V_{GE1} goes immediately from high to low. When IN1 goes from

low to high, and IN2 is low, V_{GE1} goes from low to high after a deadtime DT. If IN1 goes from low to high when IN2 is still high, V_{GE1} remains low, only when V_{GE2} goes low, V_{GE1} goes high a DT delay after the falling edge of IN2.

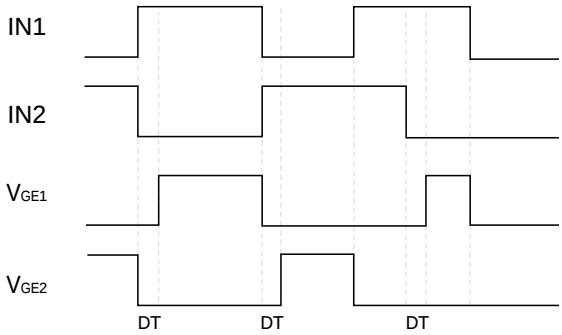


Figure 9. Transmission logic in half-bridge mode

The minimum deadtime DT is 1.6us, if pin Cx is left open. DT can be adjusted by connecting a capacitor C_{DTx} between Cx and GND(CC).

C_{DTx}[pF]	DT[µs]		C_{DTx} [pF]	DT[µs]
0	1.6		330	4.3
47	2		470	5.4
100	2.4		1000	9.6
220	3.4			

Connection to IGBT

The gate of the IGBT is connected to the GATEx pin of the driver core via external gate resistor R_{Gx}. The emitter of the IGBT is connected to the COMx pin directly. It is recommended to connected a resistor R_{GEx} (lower than 10kΩ) and clamping diodes between the gate and emitter to avoid over voltage.

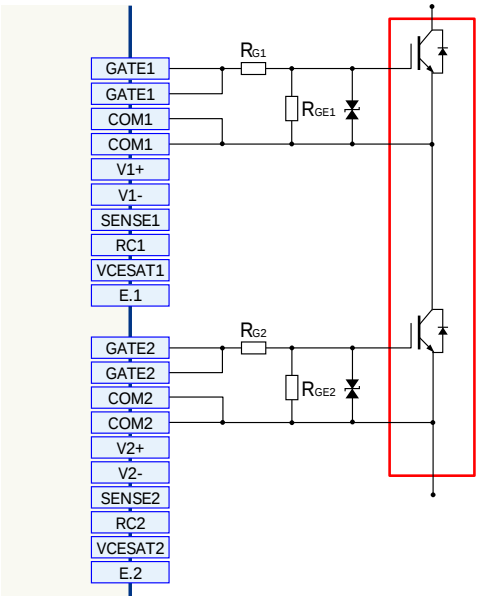


Figure 10. Connection to the IGBT

Secondary Side Blocking Capacitors

The blocking capacitors on Vx+ and Vx- are necessary to avoid voltage dip and must be placed as close as possible to the driver core. It is recommended to use additional external blocking capacitors of 220uF.

Short Circuit Protection

A comparator inside the driver compares the volage at the V_{CESATx} input with the reference voltage V_{REF}. The maximum voltage at the V_{CESATx} pin is 10V.

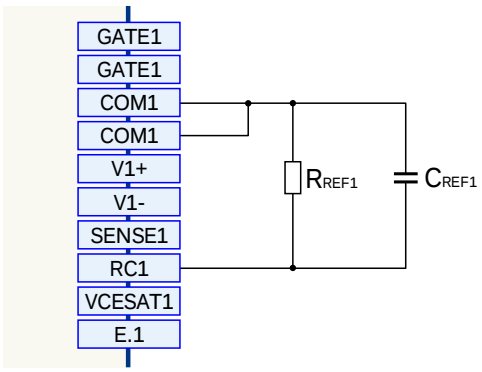


Figure 11. RC network to configure threshold reference voltage

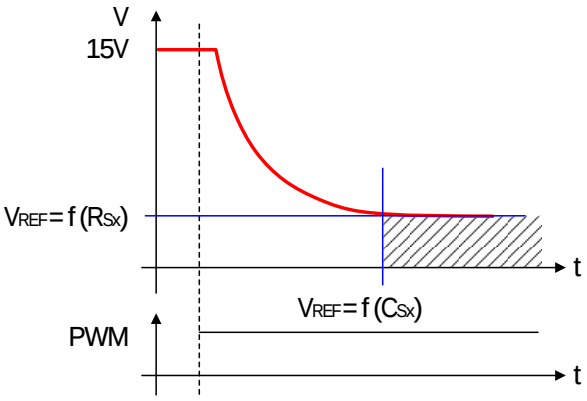


Figure 12. Reference curve

The terminal RCx allows the threshold reference to be configured for short-circuit protection with a resistor R_{REFx} placed between RCx and COMx. Instead of a static reference, a dynamic reference is used to check the collector-emitter voltage of the IGBT at turn-on. The time constant of the dynamic reference can be configured with a capacitor C_{REFx} placed between RCx and COMx. It allows the short-circuit duration elapses before an protection action to be adjusted.

The table in below shows the static reference and short circuit duration for different combinations of R_{REFx} and C_{REFx}.

Threshold reference	R_{REFx}	C_{REFx} =0	C_{REFx} =100pF	C_{REFx} =220pF	C_{REFx} =470pF	C_{REFx} =1nF
2V	2kΩ	0.5μs	1.5μs	3μs	5μs	7μs
4V	5.4kΩ	1μs	3μs	4μs	9μs	
6V	12kΩ	1μs	4μs	6μs		
8V	32kΩ	1μs	5μs	7μs		
9V	70kΩ	1μs	5μs	7μs		

It is recommended to have R_{VCEx}=470Ω and C_{VCEx}=1nF. Please be sure that the IGBT should be turned off within 10μs after the short circuit.

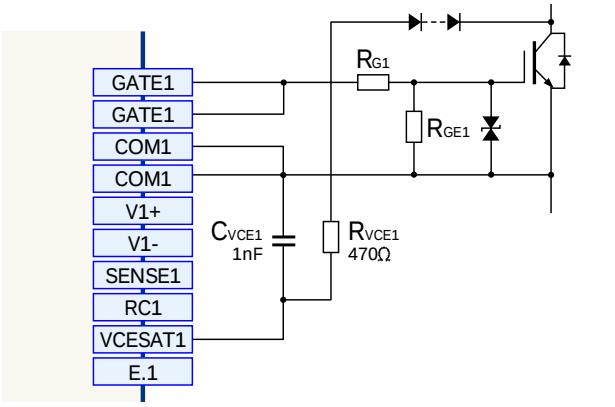


Figure 13. RC timing network for IGBT short circuit detection

Soft Shut Down

The soft shut down is used to switch off the IGBT if a fault occurs and meanwhile avoid voltage overshoot by reducing the turn-off di/dt. The value of the configuration resistor R_{SSD} has to be determined in a practical manner. IGBT modules higher input capacitance will require a lower R_{SSD}, while lower input capacitance require a higher R_{SSD}.

Note: Soft shut down may slightly increase the V_{GEx}, clamping diodes are recommended.

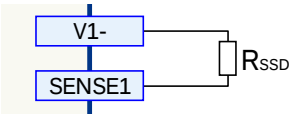


Figure 14. Configuration resistor for soft shut down

External Fault Input

The driver has inputs E.x to accept external fault signal to set the internal fault memory, so as to trigger a soft shut down. The fault inputs have an active high logic. These inputs can be used to detect an over-temperature or over-current.

Note: E.x may rise up to the potential of the DC-link's positive terminal. E.x have to be connected to COMx if unused.

Sense Input and Active Clamping

A further application of the SENSEx input is active clamping with direct feedback to the output stage. This method can be combined with the conventional active clamping which is connected to the gate of the IGBT.

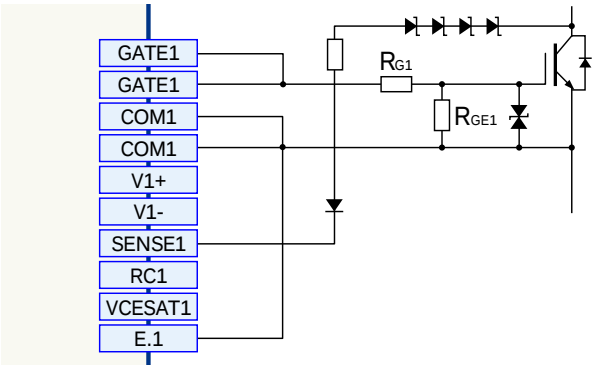


Figure 15. Circuitry for active clamping

Mechanical Dimensions

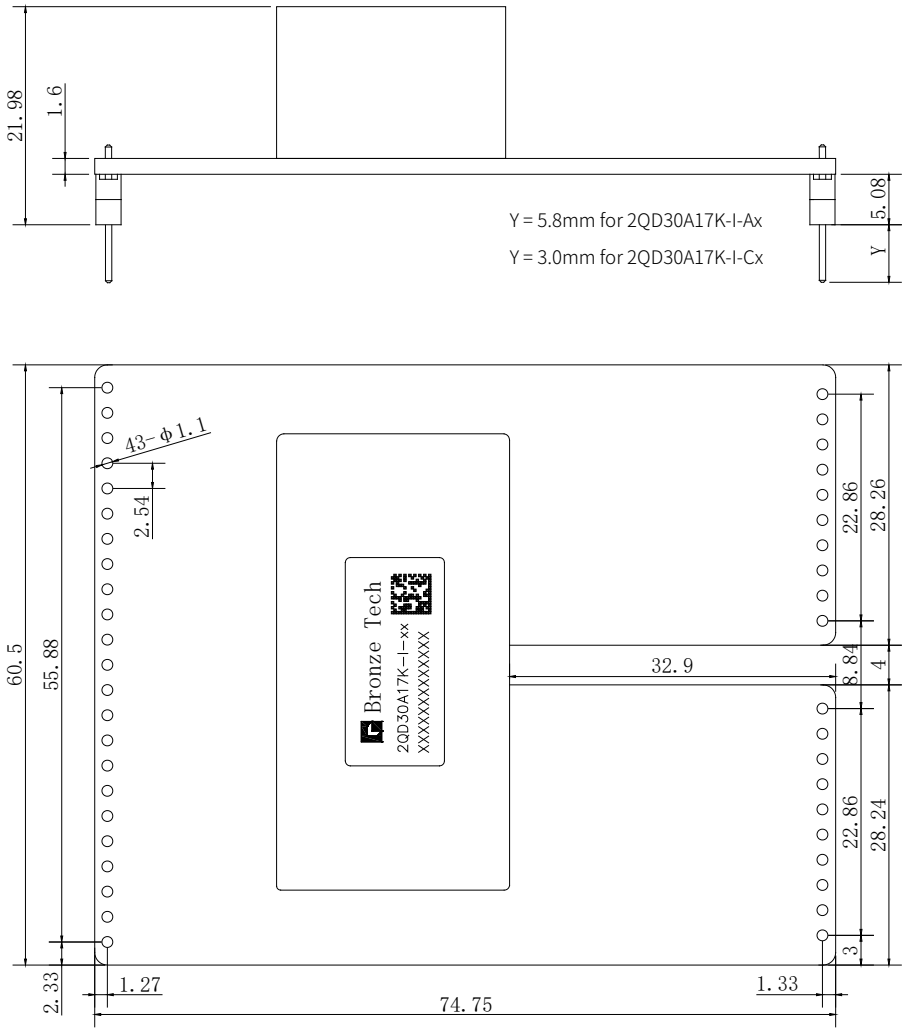


Figure 16. Mechanical drawing of 2QD30A17K-I-xx

Note: 1)Legend unit: mm.
2)The margin tolerance conforms with the ISO 2768-1.
3)The primary side and secondary side pin grid is 2.54mm with a pin cross section of 0.64mmx0.64mm. Recommended diameter of solder pads is 2mm and diameter of drill holes is 1.2mm.

Revision History

REVISION	NOTES	DATE
V1.0	Initial release	16-Apr-2024
V1.1	Update ordering information	11-Oct-2024

Precautions

- All operations on the IGBT module and driver shall conform with the electrostatic-sensitive device (ESD) protection requirements stipulated in IEC 60747-1/IX or EN100015.
- To protect ESDs, IGBT module and driver operation, including the operation sites and tools, must conform with these standards.

The IGBT and driver may be damaged due to negligence in ESD protection.

- Before powering on the driver, make sure that the driver and control board are connected correctly, without empty connection, false connection, or false soldering.
- After the driver is installed, its surface voltage to the ground may exceed the safety voltage. Therefore, do not touch it with bare hands.

Operations may involve life hazards. Be sure to follow the corresponding safety protocols !

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